Claims

[c1]   1. A non-volatile memory structure, comprising:

a substrate;

a plurality of gate structures, disposed on the substrate, wherein each substrate structure comprises, from the substrate, at least a bottom dielectric layer, a charge-trapping layer, an upper dielectric layer, a control gate and a cap layer;

a plurality of select gate structures, wherein each of the select gate structures is disposed on one side of each gate structure respectively such that the gate structures are serially connected together to form a memory cell row, wherein each select gate structure comprises, from the substrate, at least a select gate dielectric layer and a select gate;

a plurality of spacers, disposed between the gate structures and the select gate structures; and

a source/drain region, disposed in the substrate on each side of the memory cell row.

[c2]   2. The non-volatile memory structure of claim 1, wherein each of the select gate structures completely fills the space between the gate structures.

[c3]   3. The non-volatile memory structure of claim 1, wherein material constituting the charge-trapping layer comprises silicon nitride.

[c4]   4. The non-volatile memory structure of claim 1, wherein material constituting the bottom dielectric layer and the upper dielectric layer comprises silicon oxide.

[c5]   5. The non-volatile memory structure of claim 1, wherein material constituting the control gate and the select gate comprises polysilicon.

[c6]   6. The non-volatile memory structure of claim 1, wherein the select gate dielectric layer has a thickness between about 160Å to 170Å.

[c7]   7. A non-volatile memory structure, comprising:
a gate structure, having at least a bottom dielectric layer, a charge-trapping layer, an upper dielectric layer, a control gate and a cap layer over a substrate;
a select gate, disposed on one side of the gate structure;
a spacer, disposed between the gate structure and the select gate;
a select gate dielectric layer, disposed between the select gate and the substrate;
a source region, disposed in the substrate on one side of the gate structure corresponding to the select gate; and

a drain region, disposed in the substrate adjacent to the select gate.

[c8]   8. The non-volatile memory structure of claim 1, wherein material constituting the charge-trapping layer comprises silicon nitride.

[c9]   9. The non-volatile memory structure of claim 1, wherein material constituting the bottom dielectric layer comprises silicon oxide.

[c10]   10. The non-volatile memory structure of claim 1, wherein material constituting the upper dielectric layer comprises silicon oxide.

[c11]   11. A method of fabricating a non-volatile memory, comprising the steps of:
providing a substrate;
forming a plurality of gate structures on the substrate, wherein each gate structure comprises, from the substrate, a bottom dielectric layer, a charge-trapping layer, an upper dielectric layer, a control gate and a cap layer;
forming a plurality of spacers on the sidewalls of the gate structures;
forming a select gate dielectric layer over the substrate;
forming a plurality of select gates on each side of the gate structures such that the gate structures are serially

connected together to form a memory cell row;

forming a source/drain region in the substrate on each side of the memory cell row; and

forming a bit line over the substrate to electrically connect with the drain region.

[c12]   12. The method of claim 11, wherein the step of forming the gate structure over the substrate further comprises:

forming a first dielectric layer over the substrate;

forming a charge-trapping material layer over the first dielectric layer;

forming a second dielectric layer over the charge-trapping layer;

forming a first conductive layer over the second dielectric layer;

patterning the first conductive layer to form the control gate; and

patterning the second dielectric layer, the charge-trapping material layer, the first dielectric layer to form the upper dielectric layer, the charge-trapping layer and the bottom dielectric layer.

[c13]   13. The method of claim 11, wherein material constituting the charge-trapping layer comprises silicon nitride.

[c14]   14. The method of claim 11, wherein the step of forming the select gate dielectric layer over the substrate com-

prises performing a thermal oxidation process.

[c15] 15. The method of claim 11, wherein the step of forming the select gates on etch side of the gate structures comprises:

forming a second conductive layer over the substrate, wherein the second conductive layer completely fills the space between the gate structures; and

removing the gate structures and a portion of the second conductive layer disposed outside the area for forming the memory cell row.

[c16] 16. The method of claim 11, wherein the step of forming the source region/drain region in the substrate on each side of the memory cell row comprises performing an ion implantation process.

[c17] 17. The method of claim 11, wherein material constituting the charge-trapping layer comprises silicon nitride.

[c18] 18. The method of claim 11, wherein material constituting the bottom dielectric layer and the upper dielectric layer comprises silicon oxide.